UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,623	11/24/2003	Joseph P. Miller	200304072-3	4259

22879 7590 09/12/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,623	MILLER ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-26,34 and 36-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-26,34 and 36-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-26, and 34-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Begis (U.S. Patent 5,610, 801) in view of Klaser (U.S. Patent 4,870,746).

As to claims 15-23, 25, Begis discloses a system (a motherboard assembly 10) as shown in figures 1-2 for a computer system (column 1, line 17) comprising a circuit board, which is a motherboard (12, column 2, lines 20-22), the motherboard (12) comprising: a first interface (pad) coupled to a first set of traces (column 2, lines 24-26, and the motherboard inherently including pad and traces, wiring, or circuitries for electrical connection to a daughterboard or components mounted on the motherboard)., and an interstitial circuit board (24, column 2, lines 40, 44) comprising a second interface (pads or lands) coupled to the first interface (pad of the motherboard), a second set of traces (column 2, lines 42-43), and a third interface (pads or lands on a top surface of the daughterboard 24 electrically couple to an integrated circuit device, which is a processor, controller, or memory controller (26). Begis further discloses the

interstice board having multilayer including a power ad ground planes (column 2, lines 42-44).

Begis does not specific disclose the second set of traces of the interstitial circuit board having a plurality of termination components comprise a resistor disposed in multilevel of the interstice circuit board.

Klaser shows a multiplayer circuit board (8) having surface mount resistors (16) embedded within the interior of the multiplayer circuit board (8) disclosed in figures 1-2, and 4.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Klaser to employ the apparatus of Begis in order to provide a laminated structure of bonding layers together to form a multilayer circuit board and also provide a resistance value on each of bonding layers to form an impedance value of the multiplayer circuit board.

As to claim 24, Begis discloses the apparatus as shown in figures 1-2 wherein the second member (24) has a substantially smaller footprint area than the motherboard (12).

As to claim 26, Begis discloses a system (a motherboard assembly 10) as shown in figures 1-2) comprising a circuit board, which is a motherboard (12, column 2, lines 20-22), the motherboard (12) comprising: a first interface (pad) coupled to a first set of traces (column 2, lines 24-26, and a second circuit board (24, column 2, lines 40, 44) comprising a second interface (pads or lands) coupled to the first interface (pad of the motherboard), a second set of traces (column 2, lines 42-43), and a third interface (pads

or lands on a top surface of the daughterboard 24 electrically couple to an integrated circuit device (26).

Begis does not specific disclose the second traces comprising mean for reducing signal degradation.

Klaser shows a multiplayer circuit board (8) having surface mount resistors (16) embedded within the interior of the multiplayer circuit board (8) disclosed in figures 1-2, and 4.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Klaser to employ the apparatus of Begis in order to reduce noise signals.

As to claims 34, 36-39, Begis discloses a system (a motherboard assembly 10) as shown in figures 1-2 comprising an IC (a processor 22) having a first interface (pads or lands), and an interstitial circuit board (24, column 2, lines 40, 44) comprising a second interface (pads or lands) coupled to the first interface (pads of the IC 26), a second set of traces (column 2, lines 42-43), and a third interface (pads or lands on a bottom surface of the daughterboard 24) electrically couple to a circuit board (12), which is a processor, controller, or memory controller (26). Begis further discloses the interstice board having multilayer including a power ad ground planes (column 2, lines 42-44).

Begis does not specific disclose the second set of traces having a plurality of termination components comprise a resistor disposed in multilevel of the interstice circuit board.

Klaser shows a multiplayer circuit board (8) having surface mount resistors (16) embedded within the interior of the multiplayer circuit board (8) disclosed in figures 1-2, and 4.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Klaser to employ the apparatus of Begis in order to provide a laminated structure of bonding layers together to form a multilayer circuit board and also provide a resistance value on each of bonding layers to form an impedance value of the multiplayer circuit board.

Response to Arguments

3. Applicant's arguments filed 06/19/06 have been fully considered but they are not persuasive.

Applicant argues:

Begis does not disclose "a first set of traces free of termination components"

Examiner disagrees because as best understood, the phrase can be described as "the traces are not connected to the terminal components". Begis disclose the traces (not connected to) free of terminal components.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
August 29, 2006.